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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/722,110	11/25/2003	Luca De Santis	400.225US01	4849

27073 7590 08/09/2006

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EXAMINER	
TSAI, SHENG JEN	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 08/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/722,110	DE SANTIS ET AL.	
	Examiner	Art Unit	
	Sheng-Jen Tsai	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 July 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-40* is/are pending in the application.

4a) Of the above claim(s) *29 and 32-40* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28,30 and 31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is taken in response to Applicants' Amendment and Remarks filed on July 20, 2006 regarding application 10,722,110 filed on November 25, 2003.

2. Claims 29 and 32-40 have been cancelled.

Claims 1, 14, 19 and 24 have been amended.

Claims 1-28 and 30-31 are pending for consideration.

3. ***Response to Remarks and Amendments***

Applicants' amendments and remarks have been fully and carefully considered.

Each of independent claims 1, 14, 19 and 24 has been amended with the additional limitation of "**wherein the first signal is sent from the register bank to the analog/memory core without passing through the bus controller**."

In response to the amendments, claim rejections under 35 U.S.C. 102(b) as being anticipated by Sukegawa et al. (U.S. 5,603,001) and claim rejections under 35 U.S.C. 103(b) as being unpatentable over Sukegawa et al. (U.S. 5,603,001) have been withdrawn.

It is noted, however, that this newly added limitation is disclosed by Robinson (U.S. 5,937,423), as explained below.

The Examiner wrote in the Office Action mailed on 6/20/2006 that

"As to claim 1, Robinson discloses **a memory device controller** [figure 3 shows a flash memory device (27) and the associated controller (the interface, 30)] **comprising**:

an updateable register bank [a group of registers (figure 3, 32~58) comprising command register (32), status register (33), source address register (34), destination address register (35), length register (36), erase queue register (37), data I/O register (38) and data I/O register (58); all these registers are programmable (i.e., updateable) by the CPU (figure 1, 11) via the CPU/PCI Bus/Memory bridge (figure 1, 14) and the local bus (figure 1, 12)] **adapted to send a first signal** [the corresponding first signal is the address signal (address decoder, figure 3, 63)] **to an analog/memory core of the memory device** [blocks of flash EEPROM memory cells (figure 3, 68)] **for controlling operation of the analog/memory core** [column 8, lines 24-60], **the analog/memory core comprising an array of flash memory cells** [blocks of flash EEPROM memory cells (figure 3, 68)] **and supporting analog access circuitry** [For the embodiment illustrated, a first byte defines the minimum power supply voltage used with the array in its normal operating condition. A second byte defines the maximum power supply voltage used with the array in its normal operating condition. A third byte defines the minimum power supply voltage used with the array in its programming condition. A fourth byte defines the maximum power supply voltage used with the array in programming condition. The next eight bytes define various system timing parameters for different operations (column 11, lines 10-20); high voltage, figure 3, 61]; **a bus controller** [the CPU/PCI Bus/Memory bridge (figure 1, 14)] **coupled to the register bank** [via the local bus (figure 1, 12); figure 3], **the bus controller adapted to receive a second signal** [the corresponding second signal may be one of the output data (data multiplexer, figure 3, 62)] **from the register bank** [via the local bus (figure 1,

12); figure 3] **and to send a third signal** [the third signal may be the command (command register, figure 3, 32)] **to the register bank for updating the register bank** [via the local bus (figure 1, 12); figure 3, "data and command in"];

a select register [register select, figure 3, 59] **coupled to the register bank** [as shown in figure 3]; **and**

a first processor [the CPU, figure 1, 11] **coupled to the bus controller and the select register** [all these registers are programmable (i.e., updateable) by the CPU (figure 1, 11) via the CPU/PCI Bus/Memory bridge (figure 1, 14) and the local bus (figure 1, 12); figure 3]."

It is noted that, according to the above claim analysis, those elements recited in the added limitation have their correspondences in the invention by Robinson as follows:

- The corresponding first signal is the address signal (address decoder, figure 3, 63),
- The corresponding register bank is the group of registers (figure 3, 32~58) comprising command register (32), status register (33), source address register (34), destination address register (35), length register (36), erase queue register (37), data I/O register (38) and data I/O register (58),
- The corresponding analog/memory core is blocks of flash EEPROM memory cells (figure 3, 68), and
- The corresponding bus controller is the CPU/PCI Bus/Memory bridge (figure 1, 14).

It is further noted that figure 1 of Robinson shows that the CPU/PCI Bus/Memory bridge (14) and the flash memory device (18) is connected by a local bus (12), while figure 3 of Robinson shows that the register bank (figure 3, 32~58), the address signal (i.e., the first signal, (address decoder, figure 3, 63)) and the flash EEPROM memory cells (figure 3, 68) all reside inside the flash memory device (figure 1, 18). Therefore,

the transmission of the first signal from the register bank to the flash EEPROM memory cells takes place within the flash memory device without passing through the CPU/PCI Bus/Memory bridge (figure 1, 14), as clearly shown in figure 3 of Robinson.

Therefore, the Examiner's position regarding the status of claims 1, 14, 19 and 24, and those claims dependent from them, remain the same as stated in the previous Office Action.

A new iteration of claim analysis has been embarked in response to the amendments. Refer to the corresponding sections of the following claim analysis for details.

Claim Rejections - 35 USC § 102

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-4, 6-8, 11, 13-15, 17-20, 22-28 and 30-31 are rejected under 35 U.S.C. 102(b) as being anticipated by Robinson (U.S. 5,937,423).

As to claim 1, Robinson discloses **a memory device controller** [figure 3 shows a flash memory device (27) and the associated controller (the interface, 30)] **comprising**:

an updateable register bank [a group of registers (figure 3, 32~58) comprising command register (32), status register (33), source address register (34), destination address register (35), length register (36), erase queue register (37), data I/O register (38) and data I/O register (58); all these registers are programmable (i.e., updateable) by the CPU (figure 1, 11) via the CPU/PCI Bus/Memory bridge (figure 1, 14) and the local bus (figure 1, 12)] **adapted to send a first signal** [the corresponding first signal

is the address signal (address decoder, figure 3, 63)] **to an analog/memory core of the memory device** [blocks of flash EEPROM memory cells (figure 3, 68)] **for controlling operation of the analog/memory core** [column 8, lines 24-60], **the analog/memory core comprising an array of flash memory cells** [blocks of flash EEPROM memory cells (figure 3, 68)] **and supporting analog access circuitry** [For the embodiment illustrated, a first byte defines the minimum power supply voltage used with the array in its normal operating condition. A second byte defines the maximum power supply voltage used with the array in its normal operating condition. A third byte defines the minimum power supply voltage used with the array in its programming condition. A fourth byte defines the maximum power supply voltage used with the array in programming condition. The next eight bytes define various system timing parameters for different operations (column 11, lines 10-20); high voltage, figure 3, 61]; **a bus controller** [the CPU/PCI Bus/Memory bridge (figure 1, 14)] **coupled to the register bank** [via the local bus (figure 1, 12); figure 3], **the bus controller adapted to receive a second signal** [the corresponding second signal may be one of the output data (data multiplexer, figure 3, 62)] **from the register bank** [via the local bus (figure 1, 12); figure 3] **and to send a third signal** [the third signal may be the command (command register, figure 3, 32)] **to the register bank for updating the register bank** [via the local bus (figure 1, 12); figure 3, "data and command in"];

a select register [register select, figure 3, 59] **coupled to the register bank** [as shown in figure 3]; **and**

a first processor [the CPU, figure 1, 11] **coupled to the bus controller and the select register** [all these registers are programmable (i.e., updateable) by the CPU (figure 1, 11) via the CPU/PCI Bus/Memory bridge (figure 1, 14) and the local bus (figure 1, 12); figure 3];

wherein the first signal is sent from the register bank to the analog/memory core without passing through the bus controller [figure 1 of Robinson shows that the CPU/PCI Bus/Memory bridge (14) and the flash memory device (18) is connected by a local bus (12), while figure 3 of Robinson shows that the register bank (figure 3, 32~58), the address signal (i.e., the first signal, (address decoder, figure 3, 63)) and the flash EEPROM memory cells (figure 3, 68) all reside inside the flash memory device (figure 1, 18). Therefore, the transmission of the first signal from the register bank to the flash EEPROM memory cells takes place within the flash memory device without passing through the CPU/PCI Bus/Memory bridge (figure 1, 14), as clearly shown in figure 3 of Robinson; refer to "*Response to Remarks and Amendments*"].

As to claim 2, Robinson teaches that **the memory device controller of claim 1, further comprising an expression checker coupled between the first processor and the bus controller** [the expressions to be checked are stored in the query mode ROM (figure 3, 31) and the data may be read on the bus (figure 1, 12) by the processor (figure 1, 11) to determine the details of the flash memory and the type of operations that may be performed (column 9, lines 15-45); FIG. 4 also illustrates a second twelve bytes that provide a description (i.e., expression) of the system interface and are returned in response to a query command (column 10, lines 25-28)].

As to claim 3, Robinson teaches that **the memory device controller of claim 1, further comprising a transfer register** [the corresponding transfer register is the command register (figure 3, 32)] **coupled to the bus controller** [as shown in figures 1 and 3] **for receiving the third signal** [the third signal is the command (command register, figure 3, 32)] **therefrom during a first clock phase, and coupled to the register bank for transmitting the third signal thereto during a second clock phase** [The data returned may be sent to the register 38 and be clocked serially in a preordered sequence so that it may be read on the bus 12 by a processor (column 9, lines 20-23)].

As to claim 4, Robinson teaches that **the memory device controller of claim 1, further comprising a clock for sending clock signals to at least one of the first processor, the register bank, and the select register** [The data returned may be sent to the register 38 and be clocked serially in a preordered sequence so that it may be read on the bus 12 by a processor (column 9, lines 20-23)].

As to claim 6, Robinson teaches that **the memory device controller of claim 1, further comprising a controller interface coupled to the first processor** [all these registers are programmable (i.e., updateable) by the CPU (figure 1, 11) via the CPU/PCI Bus/Memory bridge (figure 1, 14) and the local bus (figure 1, 12)] **and couplable to at least one of a command user interface** [each flash EEPROM device of the array includes a command user interface (CUI) including one or more state machines (column 7, lines 31-33); the command user interface within each of the flash memory devices are typically used for erasing the blocks of cells and reading or writing

data ... (column 7, lines 41-47)] **of the memory device** [the local bus (figure 1, 12)] **and a second processor located externally of the memory device** [a second processor may be the local bus master shown in figure 1].

As to claim 7, Robinson teaches that **the memory device controller of claim 6, wherein the controller interface comprises a suspension controller for causing a suspend command received thereat to be sent to the first processor at a pre-selected time of an operating cycle of the memory device controller** [whether functions such as erase and write may be suspended, the reasons for which suspendable functions may be suspended (column 9, lines 39-41)].

As to claim 8, Robinson teaches that **the first signal comprises an address of the analog/memory core** [the corresponding first signal is the address signal (address decoder, figure 3, 63)].

As to claim 10, Robinson teaches that **the first processor** [the CPU, figure 1, 11] **comprises a storage device** [the Main Memory, figure 1, 13] **that contains one or more algorithms that include instructions for controlling operation of the memory device controller** [The system 10 illustrated includes a central processing unit ("CPU") 11 that executes the various instructions provided to control the operations of the system 10 (column 5, lines 44-66)].

As to claim 11, Robinson discloses **a memory device controller comprising: an updateable register bank adapted to send a first signal to an analog/memory core of the memory device for controlling operation of the analog/memory core** [refer to "As to claim 1"];

a bus controller coupled to the register bank, the bus controller adapted to receive a second signal from the register bank and send a third signal to the register bank for updating the register bank; a select register coupled to the register bank [refer to "As to claim 1"];

a first processor coupled to the bus controller and the select register [refer to "As to claim 1"];

an expression checker coupled between the first processor and the bus controller [refer to "As to claim 2"];

a transfer register coupled to the bus controller for receiving the third signal therefrom during a first clock phase, and coupled to the register bank for transmitting the third signal thereto during a second clock phase [refer to "As to claim 3"]; **and**

a controller interface coupled to the first processor and couplable to at least one of a command user interface [refer to "As to claim 6"] **of the memory device and a second processor located externally of the memory device** [refer to "As to claim 6"].

As to claim 13, refer to "As to claim 7" presented earlier in this Office Action.

As to claim 14, Robinson discloses **a memory device comprising**

an analog/memory core comprising an array of flash memory cells and supporting analog access circuitry [blocks of flash EEPROM memory cells (figure 3, 68)];

a memory device controller comprising:

an updateable register bank adapted to send a first signal to the analog/memory core for controlling operation of the analog/memory core [refer to "As to claim 1"];
a bus controller coupled to the register bank, the bus controller adapted to receive a second signal from the register bank and send a third signal to the register bank for updating the register bank [refer to "As to claim 1"];
a select register coupled to the register bank [refer to "As to claim 1"]; **and**
a first processor coupled to the bus controller and the select register [refer to "As to claim 1"];
wherein the first signal is sent from the register bank to the analog/memory core without passing through the bus controller [figure 1 of Robinson shows that the CPU/PCI Bus/Memory bridge (14) and the flash memory device (18) is connected by a local bus (12), while figure 3 of Robinson shows that the register bank (figure 3, 32~58), the address signal (i.e., the first signal, (address decoder, figure 3, 63)) and the flash EEPROM memory cells (figure 3, 68) all reside inside the flash memory device (figure 1, 18). Therefore, the transmission of the first signal from the register bank to the flash EEPROM memory cells takes place within the flash memory device without passing through the CPU/PCI Bus/Memory bridge (figure 1, 14), as clearly shown in figure 3 of Robinson; refer to "*Response to Remarks and Amendments*"]; **and**
a command user interface coupled to the first controller and couplable to a second processor located externally of the memory device [refer to "As to claim 6"].

As to claim 15, refer to "As to claim 2" presented earlier in this Office Action.

As to claim 17, refer to "As to claim 7" presented earlier in this Office Action.

As to claim 18, Robinson discloses **a memory device comprising an analog/memory core comprising an array of flash memory cells and supporting analog access circuitry** [blocks of flash EEPROM memory cells (figure 3, 68)];

a memory device controller comprising:

an updateable register bank adapted to send a first signal to the analog/memory core for controlling operation of the analog/memory core [refer to "As to claim 1"];

a bus controller coupled to the register bank, the bus controller adapted to receive a second signal from the register bank and send a third signal to the register bank for updating the register bank [refer to "As to claim 1"];

a select register coupled to the register bank [refer to "As to claim 1"]; **and**

a first processor coupled to the bus controller and the select register [refer to "As to claim 1"];

an expression checker coupled between the first processor and the bus controller [refer to "As to claim 2"];

a transfer register coupled to the bus controller for receiving the third signal therefrom during a first clock phase, and coupled to the register bank for transmitting the third signal thereto during a second clock phase [refer to "As to claim 3"]; **and**

a command user interface coupled to the first controller and couplable to a second processor located externally of the memory device [refer to "As to claim 6"].

As to claim 19, refer to "As to claim 1" and "As to claim 18" presented earlier in this Office Action.

As to claim 20, refer to "As to claim 2" presented earlier in this Office Action.

As to claim 22, refer to "As to claim 7" presented earlier in this Office Action.

As to claim 23, refer to "As to claim 3" presented earlier in this Office Action.

As to claim 24, Robinson teaches **a method of operating a memory device controller** [Register Interface for Flash EEPROM Memory Arrays (title)], **the method comprising**:

receiving first data [the corresponding first data is the DATA OUT provided by the Data Multiplexer, figure 3, 62] **at a bus controller** [the corresponding bus controller is the CPU/PCI Bus/Memory Bridge, figure 1, 14] **of the memory device controller** [figure 1, 10] **from a first register** [any of the Data I/O registers, figure 3, 38~58] **of a register bank** [the corresponding register bank is the group of registers (figure 3, 32~58) comprising command register (32), status register (33), source address register (34), destination address register (35), length register (36), erase queue register (37), data I/O register (38) and data I/O register (58)] **of the memory device controller** [figure 1, 10];

sending second data [the corresponding second data is the COMMAND (data) IN, figure 3] **from the bus controller** [the corresponding bus controller is the CPU/PCI Bus/Memory Bridge, figure 1, 14] **to the first or a second register** [the corresponding

second register is the COMMAND registers, figure 3, 32] **of the register bank** [the corresponding register bank is the group of registers (figure 3, 32~58) comprising command register (32), status register (33), source address register (34), destination address register (35), length register (36), erase queue register (37), data I/O register (38) and data I/O register (58)] **for updating the register bank** [to update the content of the COMMAND registers]; **and**

sending a control signal [the corresponding control signal is the ERASE signal to erase blocks of cell of the Flash EEPROM Memory Cells (figure 3, 68; column 7, lines 42-47); another example of the control signal is QUERRY command (column 9, lines 5-24)] **from a third register** [the corresponding third register is the ERASE QUEUE register, figure 3, 37; or the STATUS register (figure 3, 33) which holds the query results (column 9, lines 5-24)] **of the register bank** [the corresponding register bank is the group of registers (figure 3, 32~58) comprising command register (32), status register (33), source address register (34), destination address register (35), length register (36), erase queue register (37), data I/O register (38) and data I/O register (58)] **to an analog/memory core** [the corresponding control signal is the ERASE signal to erase blocks of cell of the Flash EEPROM Memory Cells (figure 3, 68; column 7, lines 42-47)] **of the memory device** [figure 1, 10] **for controlling operation of the analog/memory core** [the corresponding control signal is the ERASE signal to erase blocks of cell of the Flash EEPROM Memory Cells (figure 3, 68; column 7, lines 42-47)], **the analog/memory core comprising an array of flash memory cells and supporting analog access circuitry** [Flash EEPROM Memory Cells (figure 3, 68); For the

embodiment illustrated, a first byte defines the minimum power supply voltage used with the array in its normal operating condition. A second byte defines the maximum power supply voltage used with the array in its normal operating condition. A third byte defines the minimum power supply voltage used with the array in its programming condition. A fourth byte defines the maximum power supply voltage used with the array in programming condition. The next eight bytes define various system timing parameters for different operations (column 11, lines 10-20); high voltage, figure 3, 61];

wherein the control signal [the corresponding control signal is the ERASE signal to erase blocks of cell of the Flash EEPROM Memory Cells (figure 3, 68; column 7, lines 42-47)] **is sent from the third register** [the corresponding third register is the ERASE QUEUE register, figure 3, 37] **of the register bank to the analog/memory core without passing through the bus controller** [figure 1 of Robinson shows that the CPU/PCI Bus/Memory bridge (14) and the flash memory device (18) is connected by a local bus (12), while figure 3 of Robinson shows that the register bank (figure 3, 32~58), the address signal (i.e., the first signal, (address decoder, figure 3, 63)) and the flash EEPROM memory cells (figure 3, 68) all reside inside the flash memory device (figure 1, 18). Therefore, the transmission of the first signal from the register bank to the flash EEPROM memory cells takes place within the flash memory device without passing through the CPU/PCI Bus/Memory bridge (figure 1, 14), as clearly shown in figure 3 of Robinson; refer to "*Response to Remarks and Amendments*"].

As to claim 25, Robinson teaches that **the method of claim 24, further comprising processing the first data at the bus controller to produce the second**

data [figure 1 shows that the data provided by the Flash Memory Device (18) needs to be processed by the bus controller (i.e., the CPU/PCI Bus/Memory Bridge, figure 1, 14) and forwarded to the CPU before the second data can be sent back to the Flash Memory Device].

As to claim 26, Robinson teaches that **the method of claim 25, wherein processing the first data at the bus controller is in response to receiving a signal from a processor of the memory device controller** [figure 1 shows that the data provided by the Flash Memory Device (18) needs to be processed by the bus controller (i.e., the CPU/PCI Bus/Memory Bridge, figure 1, 14) and forwarded to the CPU before the second data can be sent back to the Flash Memory Device; The high level device driver software 26 uses a unique query command that the central processor or other bus master may cause to be written by the drivers to the command decoder 60 (column 9, lines 9-12)].

As to claim 27, Robinson teaches that **the method of claim 25, wherein processing the first data at the bus controller comprises processing the first data in combination with third data received at the bus controller from a processor of the memory device controller from a processor** [The high level device driver software 26 uses a unique query command that the central processor or other bus master may cause to be written by the drivers to the command decoder 60 (column 9, lines 9-12)].

As to claim 28, the scenario described in "As to claim 24" is executed in a sequence of steps with the results from the preceding step triggers the next step. Since

the apparatus of Robinson's invention is a digital device, it implies that the sequence of operations is timing driven [The next eight bytes define various system timing parameters for different operations (column 11, lines 19-20)].

As to claim 30, Robinson teaches that **the method of claim 24, further comprising receiving an input signal at a third register of the register bank from the analog/memory core, the third signal indicative of operation of the analog/memory core** [figure 3 shows that the Flash EEPROM core also includes a Query Mode ROM (31) that provides operation related information regarding the Flash EEPROM (column 9, lines 15-24)].

As to claim 31, Robinson teaches that **the method of claim 24, further comprising receiving a control signal at a select register** [figure 3, 59] **of the memory device controller from a processor** [the CPU (figure 1, 11)] **of the memory device controller before receiving the first data at the bus controller for selecting the first register** [The high level device driver software 26 uses a unique query command that the central processor or other bus master may cause to be written by the drivers to the command decoder 60 (column 9, lines 9-12)].

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Robinson (U.S. 5,937,423).

As to claim 5, Robinson does not mention that **the clock comprises four clock phases.**

However, Robinson teaches that the data returned may be sent to the register 38 and be clocked serially in a preordered sequence so that it may be read on the bus 12 by a processor (column 9, lines 20-23), which implies that a series of clocks are used to facilitate the operations. The exact number of clocks, be it three, four or five, may vary depending each operations and lacks patentable significance.

7. Claims 9, 12, 16 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Robinson (U.S. 5,937,423), and in view of Ratcliff (US 4,797,876).

As to claims 9, 12, 16 and 21, Robinson does not teach that **the bus controller comprises an arithmetic logic unit adapted to perform at least one arithmetic operation on at least one of the second signal and data received from the first processor**.

However, the corresponding bus controller in Robinson's invention is a bridge, and it is well known in the art that bridge devices are commonly equipped with an arithmetic logic unit to perform arithmetic operations in order to support various bus protocols.

Further, Ratcliff discloses in the invention "Conferencing Bridge" a bridge (i.e., the corresponding bus controller) that includes an arithmetic logic unit [Referring to FIG. 2, the conference bridge 10 contains PCM input and output modules 18 and 20.

The conferencing bridge 10 also includes a speech RAM 22, a command RAM 24, a counter 26, a control interface 28 and an arithmetic logic unit 30 (column 5, lines 38-42)] that performs at least one arithmetic operation [The arithmetic logic unit 30 performs the arithmetic operations required to implement the conferencing algorithm (column 5, lines 59-62)].

Therefore, it would have been obvious foe one of ordinary skills in the art at the time of Applicants' invention to recognize that bridge devices are commonly equipped with an arithmetic logic unit to perform arithmetic operations in order to support various functions, as demonstrated by Ratcliff, thus lacking patentable significance.

8. ***Related Prior Art of Record***

The following list of prior art is considered to be pertinent to applicant's invention, but not relied upon for claim analysis conducted above.

- Robinson et al., (US 5,544,356), "Block-Erasable Non-Volatile Semiconductor memory Which Tracks and Stores the Total Number of Write/Erase Cycles for Each block."
- Sukegawa et al., (US 5,603,001), "Semiconductor Disk system Having a Plurality of Flash memories."
- Norman, (US 5,754,567), "Write Reduction in Flash Memory Systems through ECC Usage."
- Ideta, (US 6,038,635), "Microprocessor Containing Flash EEPROM Therein."
- Gelke et al., (US 6,735,661), "Integrated Circuit with Flash Memory including Dedicated Flash Bus and Flash Brideg."

- Zook, (US 5,668,976), "Error Correction Method and Apparatus for Disk Drive Emulator."
- Hasbun, (US 5,671,388), "Method and Apparatus for Performing Write Operations in Multi-Level Cell Storage Device."

Conclusion

9. Claims 1-28 and 30-31 are rejected as explained above.

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sheng-Jen Tsai whose telephone number is 571-272-4244. The examiner can normally be reached on 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sheng-Jen Tsai
Examiner
Art Unit 2186

August 1, 2006

PIERRE BATAILLE
PRIMARY EXAMINER
8/2/08